Eval Kit Manual

TDC-GPX2

Standard Board

GPX2-EVA-KIT

Content Guide

1 Introduction

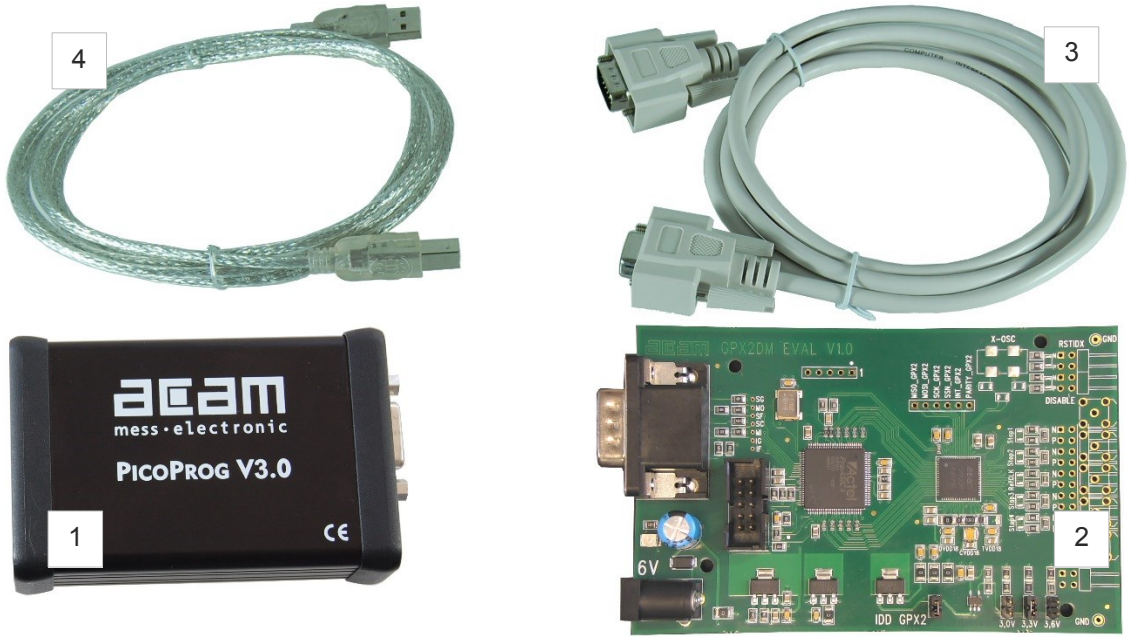
The GPX2-EVA-KIT evaluation system is designed as a platform for a quick and easy start of evaluation of the TDC-GPX2 time-to-digital converter. The kit offers a graphical user interface for user-friendly configuration and extensive testing of the TDC-GPX2.

For a proper use of the evaluation system, we strongly recommended to refer to the latest TDC-GPX2 datasheet.

Features are:

- PC supported system with USB communication interface
- Easy to use evaluation and measurement software
- Different power options, selectable by jumpers
- Three reference clock sources for alternate clock options
- Data collection to ASCII text files
- Visualization of measurement results

Figure 1: Kit Content



Pos.	Item	Comment
1	PICOPROG V3.0	Programmer and interface
2	GPX2-EVA BOARD	Based on TDC-GPX2
3	High density DSUB15 cable	Connecting Evaluation board to programmer
4	USB cable	Connects PicoProg V3.0 to PC

Please download the latest software for the kit from

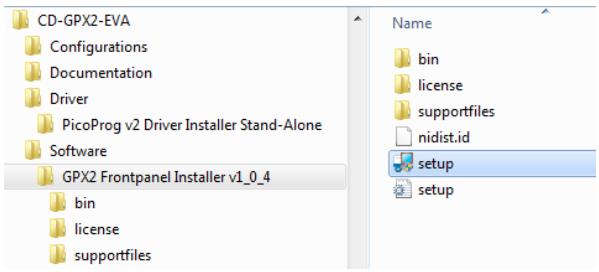
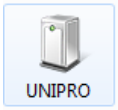
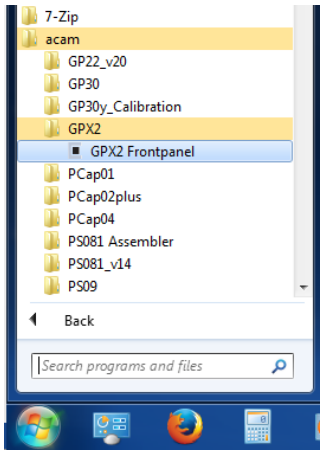
http://www.acam.de/download-center/tdc/

2 Quick Start Guide

This section describes how to set up the GPX2-EVA-KIT, establish basic operation and make measurements quickly.

2.1 Install the Software

It is crucial to install the software before connecting the evaluation kit to your computer. A default driver loading of your OS may interfere with correct installation.

Download the latest software installation package to the desired directory. Unzip the package to the desired directory. Open “setup.exe” from the unzipped directory. Follow the instructions on the screen.	
When connecting the PicoProg to the USB port it will be listed first as “picoprog v2.0 unprogrammed” device. This is true also for PicoProg V3.0.	
Starting the software will download a special firmware into the PICOPROG, picoprog_gpx2_v005.hex or higher, and the device will now be listed as “UNIPRO”:	
Open the START Menu and open the software from acam/GPX2/GPX2 Frontpanel	

2.2 Install the Hardware:

- Make sure software is installed correctly before proceeding with this step!
- Connect your computer with the PicoProg V3.0 using USB cable.
- Connect PicoProg V3.0 and the evaluation kit motherboard using the DB15 interfaces or directly.

- Connect the power supply. Make sure it is set to 6 V supply voltage.
- The green LED on the evaluation kit should be on.
- Connect your signal source.

2.3 Software

- Excecute the GPX2 Frontpanel software. The communication status should be green
- The software starts with an initial configuration, that can be opened the default configuration file config_default.cfg.
- Press “Power On Reset! – “Write Config” – “Init Reset”
- Press “Start Measurement”

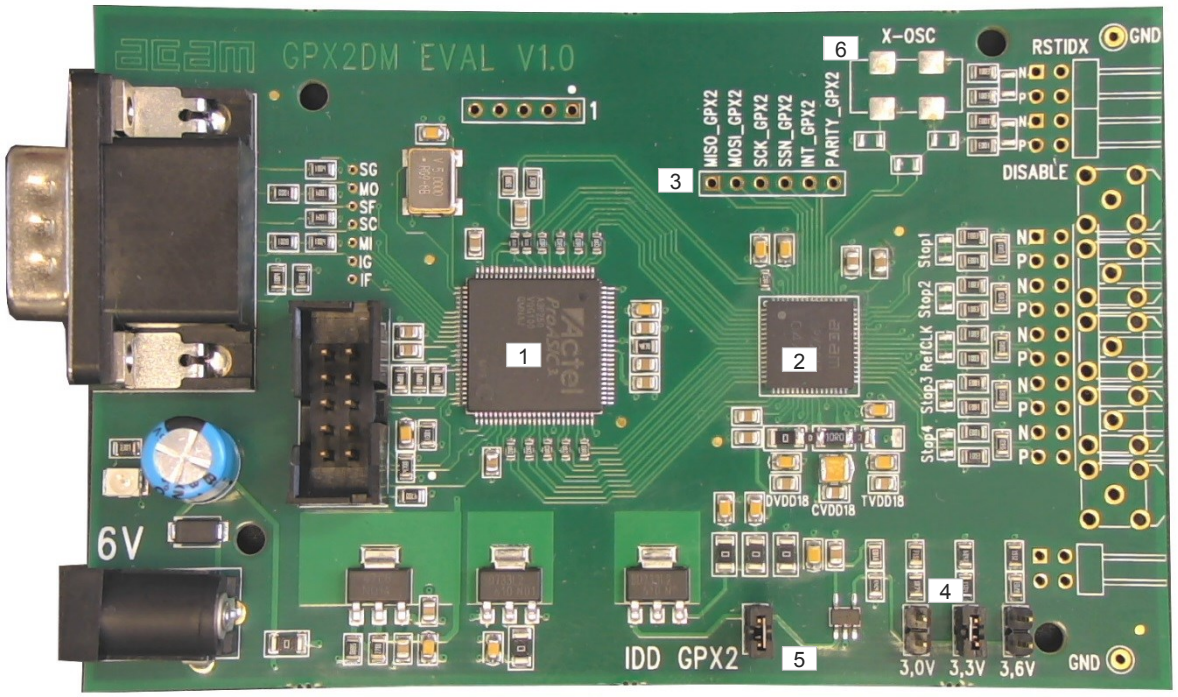
The measurement should run and results should be displayed now.

3 Hardware Description

3.1 Introduction

An on-board FPGA [1] manages the communication to the TDC-GPX [2]. It writes the configuration into the chip via the SPI interface and can use the same to read data. In addition, the FPGA manages the readout from the serial LVDS outputs of the TDC-GPX2. The SPI signals are available via additional pads [3]. A jumper selects the supply voltage as 3.0 V, 3.3 V or 3.6 V [4]. A separate jumper allows measuring the current into the TDC-GPX2 [5].

Figure 2: GPX2-EVA BOARD



Solder pads are prepared to apply an external oscillator. This may be used as a reference instead of the RefClk input.

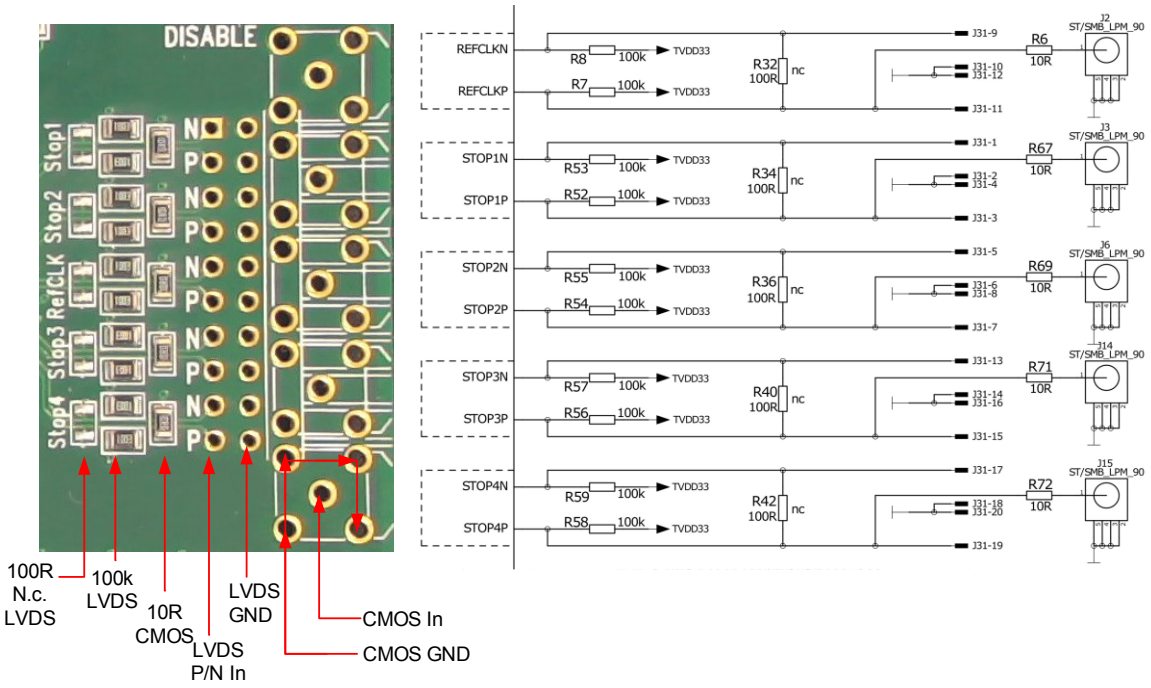
Further, solder pads are available to connect the signal lines. Here the user may solder cables directly, apply pin connectors, or in case of CMOS signals pads for SMB connectors are prepared.

Note: The FPGA manages the SPI communication and blocks the lines. Therefore, it is not possible to use the SPI for communication between an external device and TDC-GPX2.

3.2 Input Signals lines

The board is prepared to connect directly CMOS input signals or LVDS signals.

Figure 3: Input section



3.2.1 CMOS Inputs

On the board there is a 10 Ohm series resistor.

3.2.2 LVDS Inputs

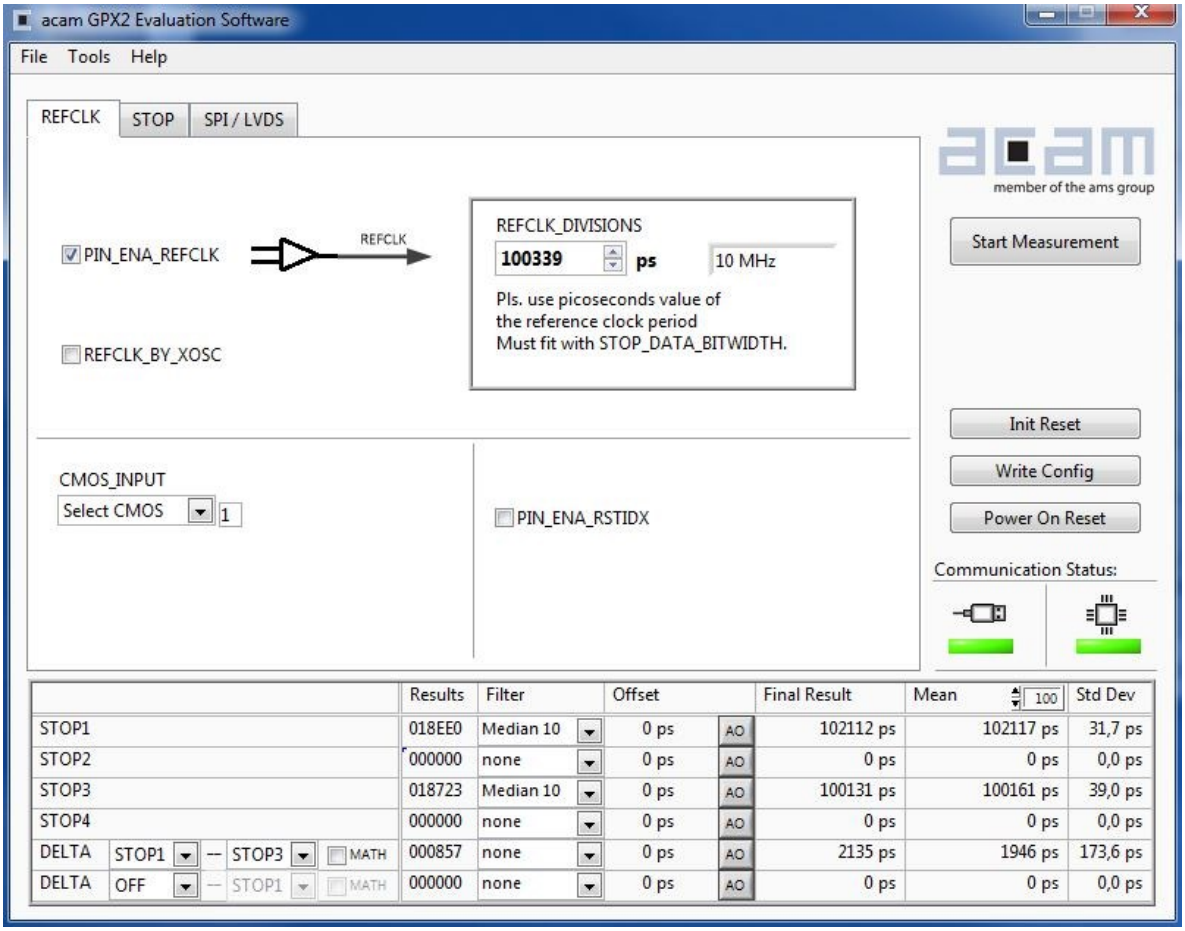
On the board there are 100kOhm pull-up resistors to TVDD33. The resistors interconnecting P and N inputs are not assembled.

4 Software Description

4.1 Main Window, REFCLK Page

The software start with the following main window:

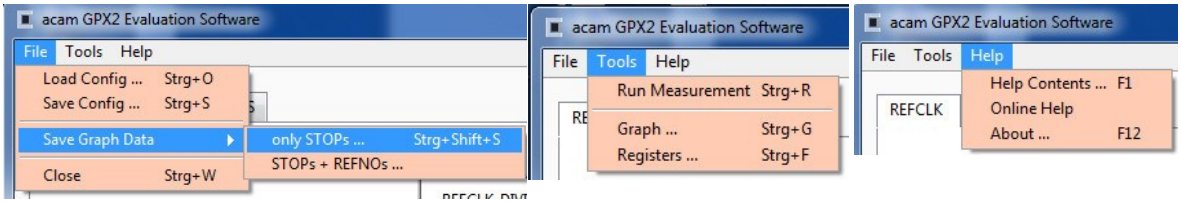
Figure 4: GPX2 evaluation software main window



The main menu offers the typical functions to load and save configurations, to run a measurement, to open the graph and register windows as well as a help.

The two figures on the right indicate the communication status. Both bar indicators should be green.

Figure 5: Menu selections



As a first step we recommend to load the standard configuration config_default.cfg, then press “Power On Reset”, “Write Config” and “Init Reset”.

The first page, “REFCLK”, allows to select the reference input as well as the definition of the LSB. REFCLK_DIVISIONS defines the LSB at the output interface as fraction of the reference clock period. The most convenient way is applying an LSB of 1ps by configuring REFCLK_DIVISIONS to the picosecond value of the reference clock period.

In the middle section the user selects between CMOS and LVDS.

At the bottom, visible on all tabulators, is the numerical display of the measurement results STOP1 to STOP2. In addition, the software allows to calculate the difference between two stop results. The select box “Math” defines the formula:

Calculation Formula:

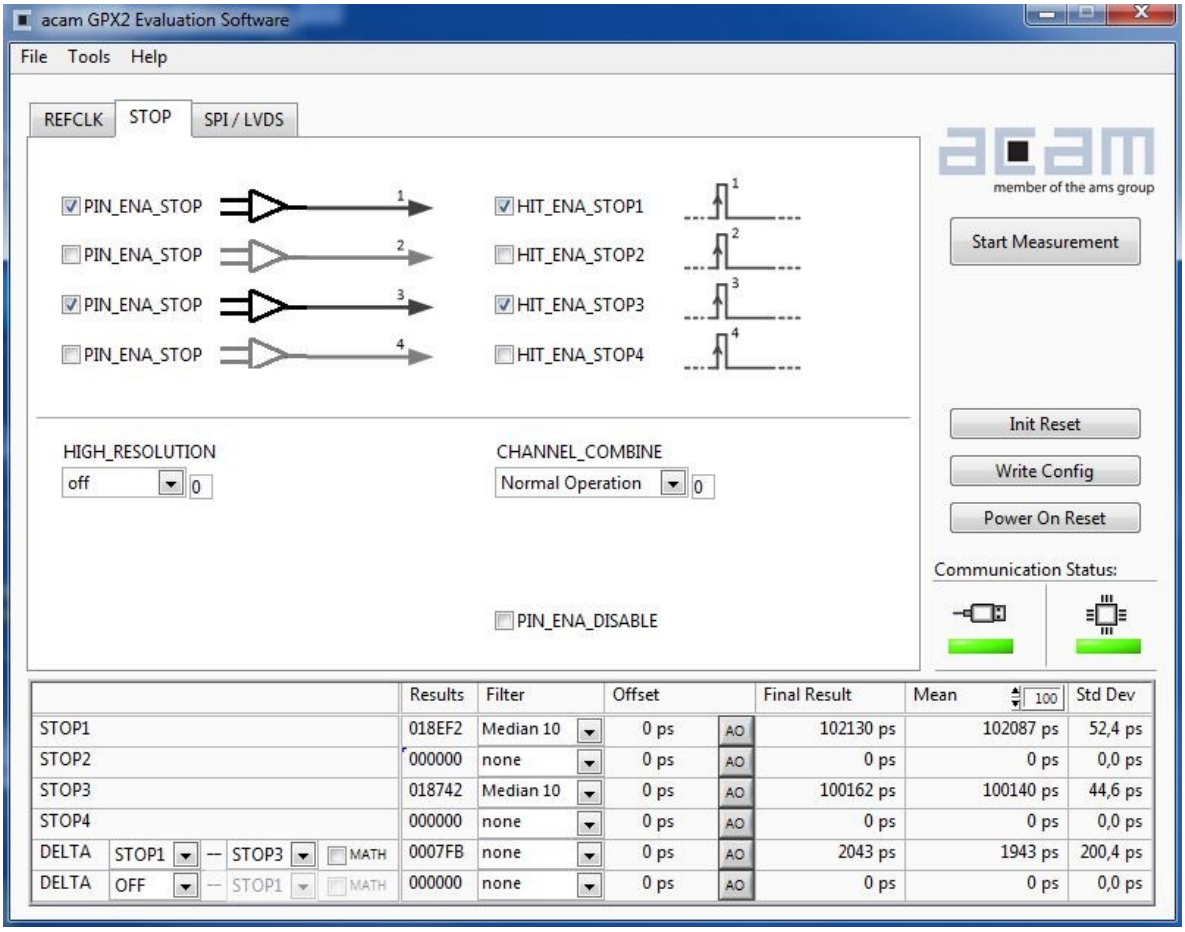
- On: [STOP1 - STOP2]
- Off: [REFNO1 - REFNO2] * REFCLK_DIVISIONS + [STOP1 - STOP2]

Various software filters, sinc or median, can be applied.

4.2 STOP Page

This page is for the PIN and HIT enable selection as well as the high resolution and combined channel settings.

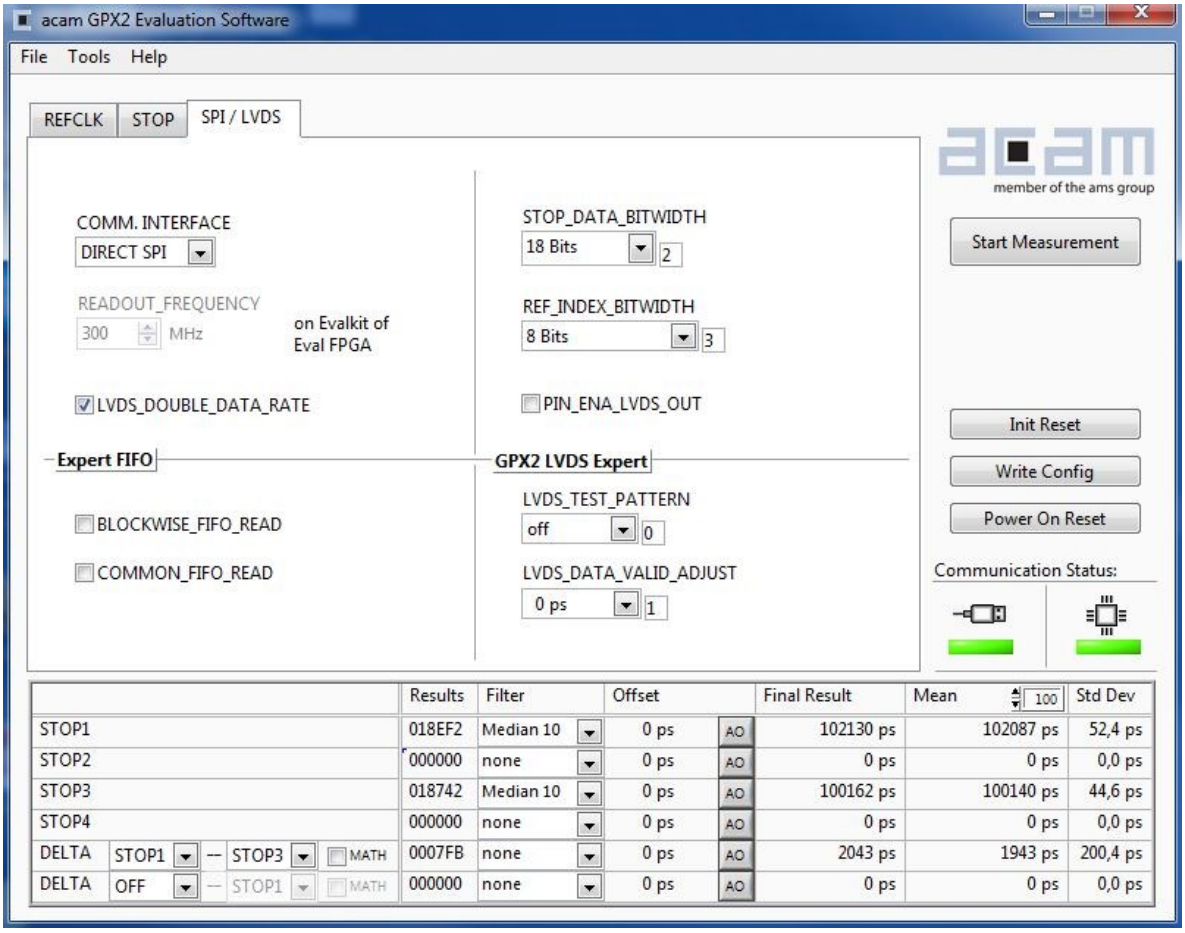
Figure 6: STOP Page



4.3 Interface Page

On this page the communication as well as the output data format is defined. In any case, on the evaluation kit all communication is done via the on-board FPGA.

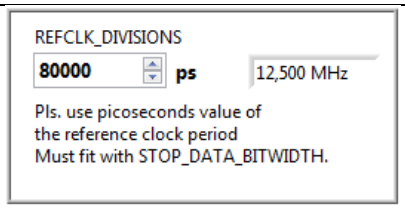
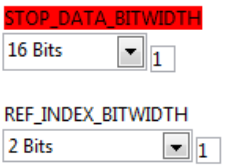
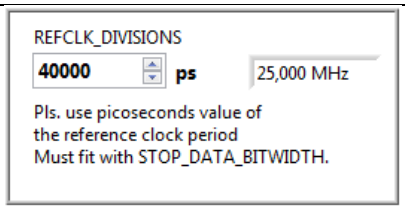
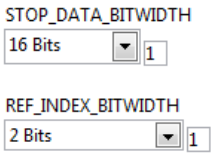
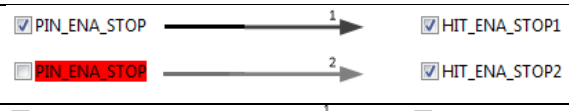
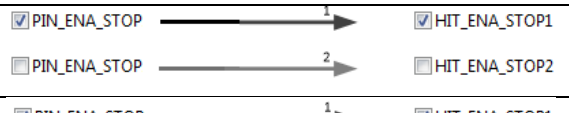
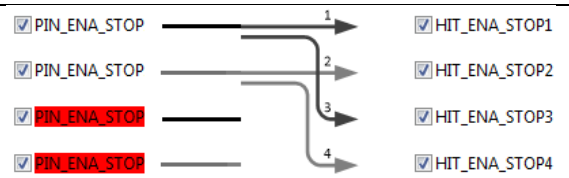
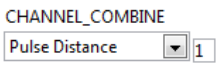
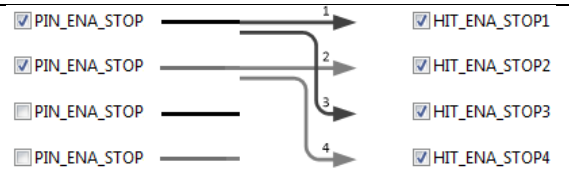
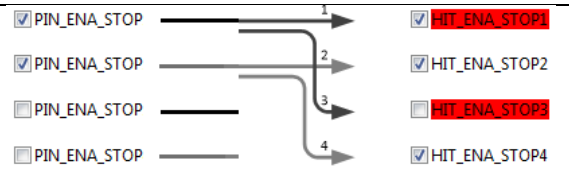
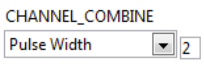
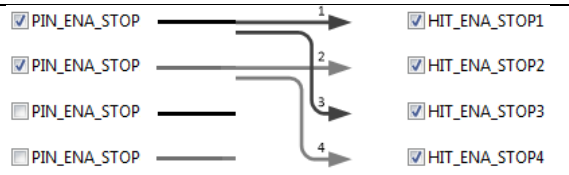
Figure 7: Kit Content



4.4 Avoiding Configuration Conflicts

Some combinations of parameter settings can prohibit operation or cause erroneous results. Some of these combinations are indicated with a red bar. User should avoid such configurations since the results may be difficult to interpret or faulty at all.

Some examples of configuration conflicts:

<table>
<tr><td rowspan="2">A</td><td>Bad</td><td> 
</td><td> 
</td></tr>
<tr><td>Good</td><td> 
</td><td> 
</td></tr>
<tr><td rowspan="2">B</td><td>Bad</td><td colspan="2"> 
</td></tr>
<tr><td>Good</td><td colspan="2"> 
</td></tr>
<tr><td rowspan="2">C</td><td>Bad</td><td> 
</td><td rowspan="2"> 
</td></tr>
<tr><td>Good</td><td> 
</td></tr>
<tr><td rowspan="2">D</td><td>Bad</td><td> 
</td><td rowspan="2"> 
</td></tr>
<tr><td>Good</td><td> 
</td></tr>
<tr><td>E</td><td></td><td>The LVDS readout frequency is recommended up to 360MHz in SDR mode only. Nevertheless 400 MHz is possible to configure and operate</td><td> 
</td></tr>
</table>

4.5 Register Content

A separate window shows the register content in the GUI and the TDC-GPX2. Separate pages display configuration data and result data. Changing the hexadecimal values will change the configuration in the GUI accordingly. With “Write Config” the updated configuration is downloaded into the chip.

Figure 8: Registers Window: Configuration

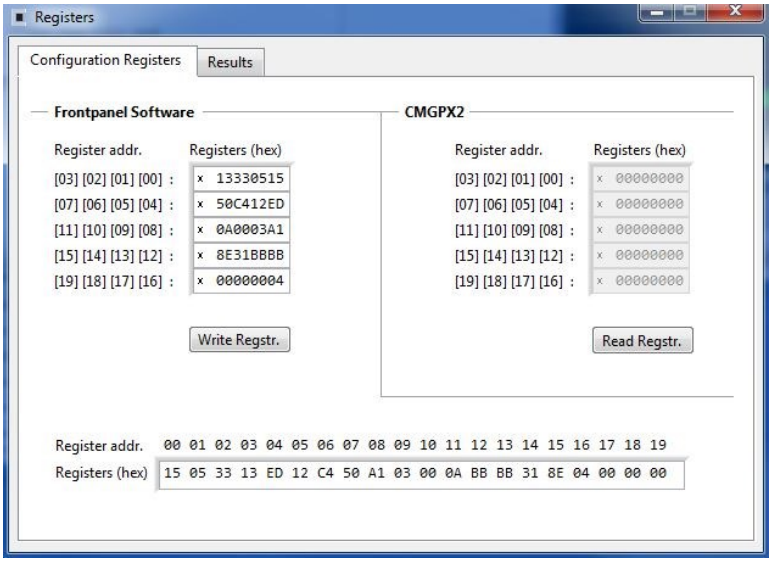
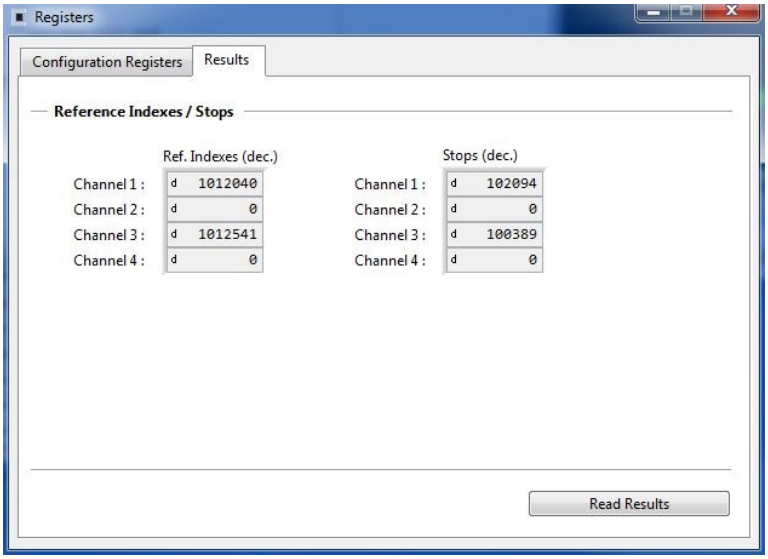


Figure 9: Registers Window: Results

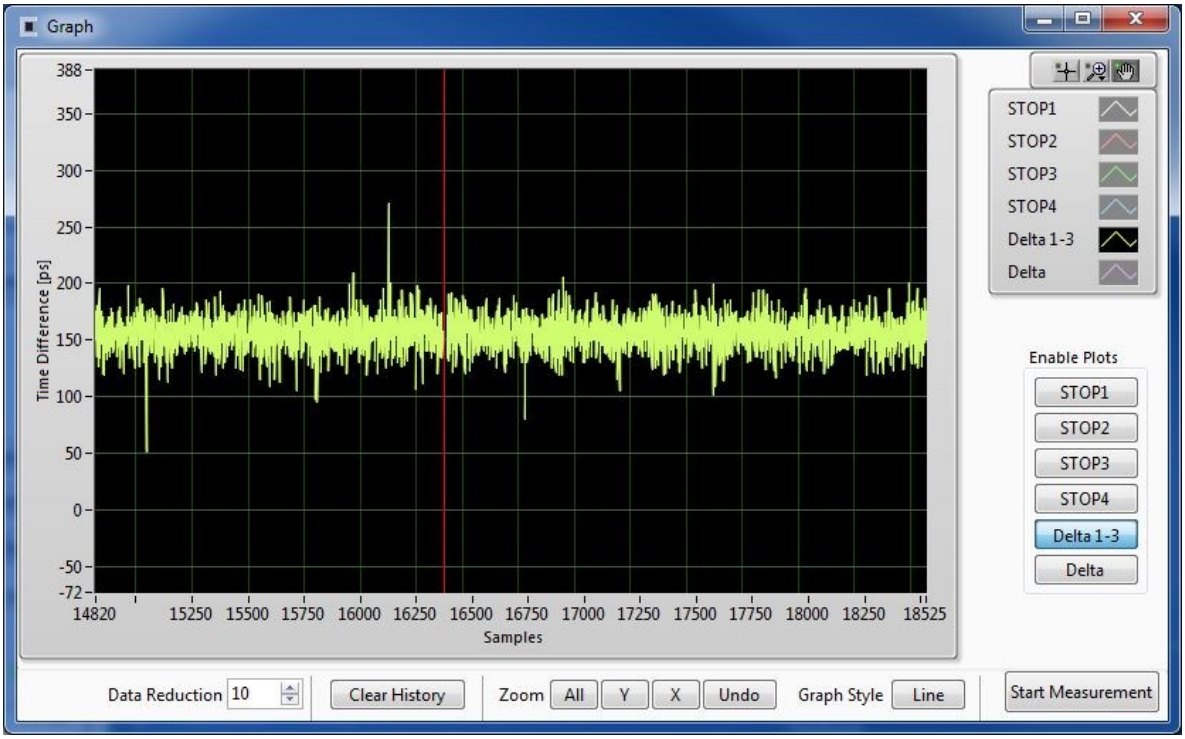


4.6 Graph Window

The graphical display allows to select which data shall be displayed. The shape of the individual curves can be modified individually. Move the mouse over the line symbol and press the right mouse button. A menu with many options will pop up.

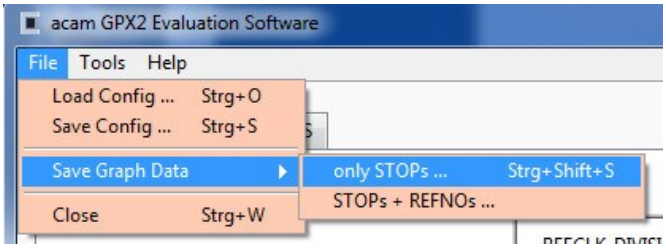
There are dedicated buttons for zoom to all or zoom in X or Y only. In addition, the standard Labview zoom functions are available (see the icons on the top right).

Figure 10: Graph Window



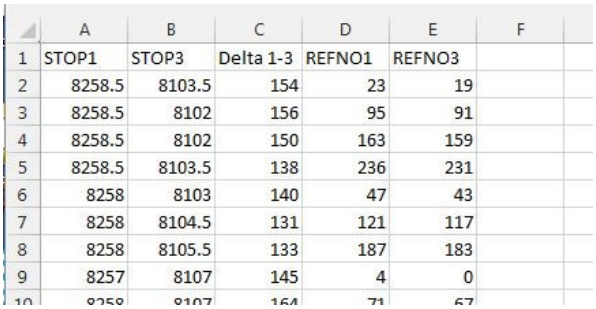
The displayed data can be exported into a text file. The maximum is 128,000 data sets.

Figure 11: Save data menu



The text file can then be analized with a table calcluation program.

Figure 12: Exported data format



	A	B	C	D	E	F
1	STOP1	STOP3	Delta 1-3	REFNO1	REFNO3	
2	8258.5	8103.5	154	23	19	
3	8258.5	8102	156	95	91	
4	8258.5	8102	150	163	159	
5	8258.5	8103.5	138	236	231	
6	8258	8103	140	47	43	
7	8258	8104.5	131	121	117	
8	8258	8105.5	133	187	183	
9	8257	8107	145	4	0	

4.7 Known Errors

- Software Hang-up
  - Once in a while, typically during tests in the temperature chamber, it may happen that the software hangs up. This is most likely to erroneous reading from the FIFO and related in the FPGA. The error will be removed in the next revision of the FPGA.
  - Workaround: restart the software.

5 Schematics, Layers and BOM

Figure 13: GP30-EVA BOARD Schematics 1

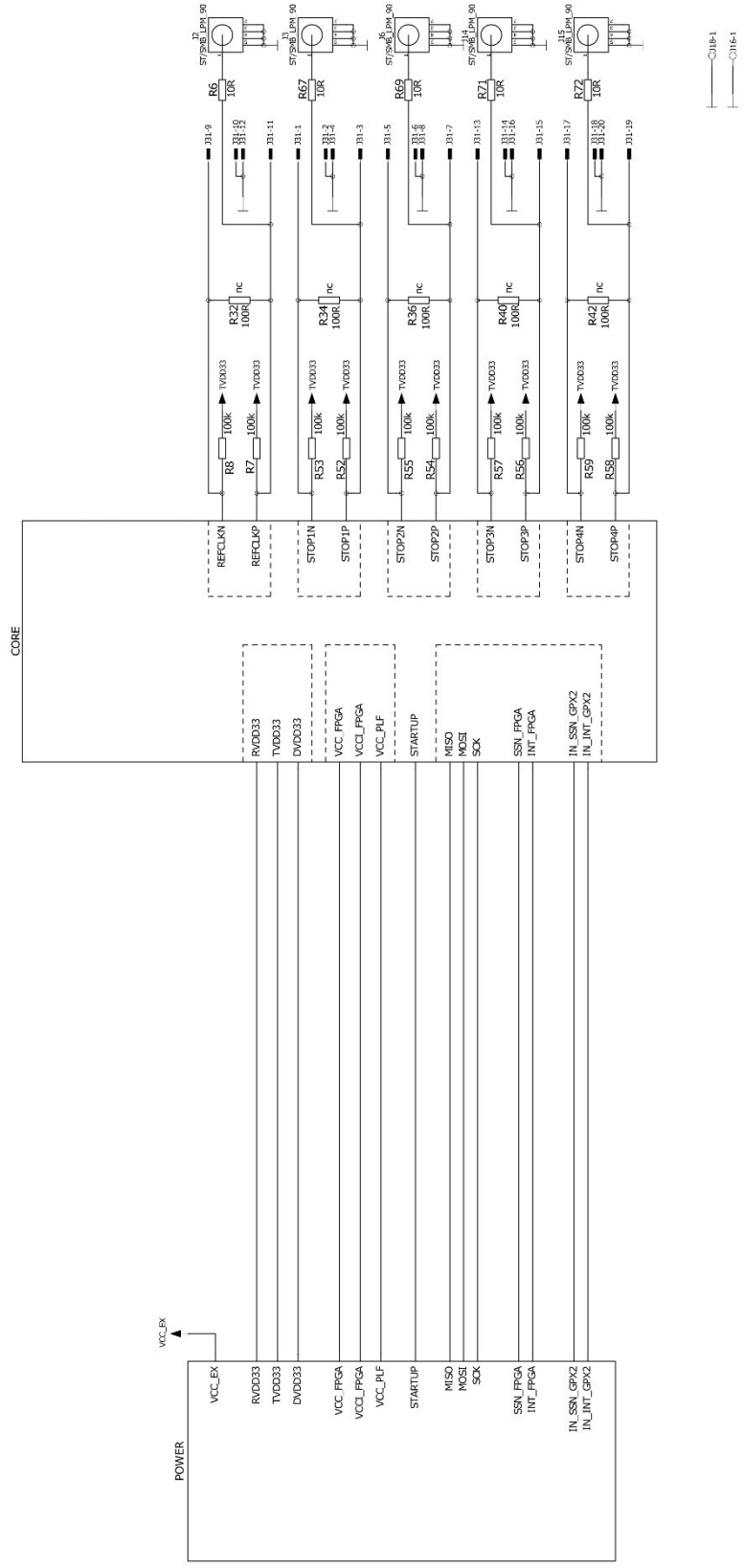


Figure 14: GP30-EVA BOARD Schematics 2

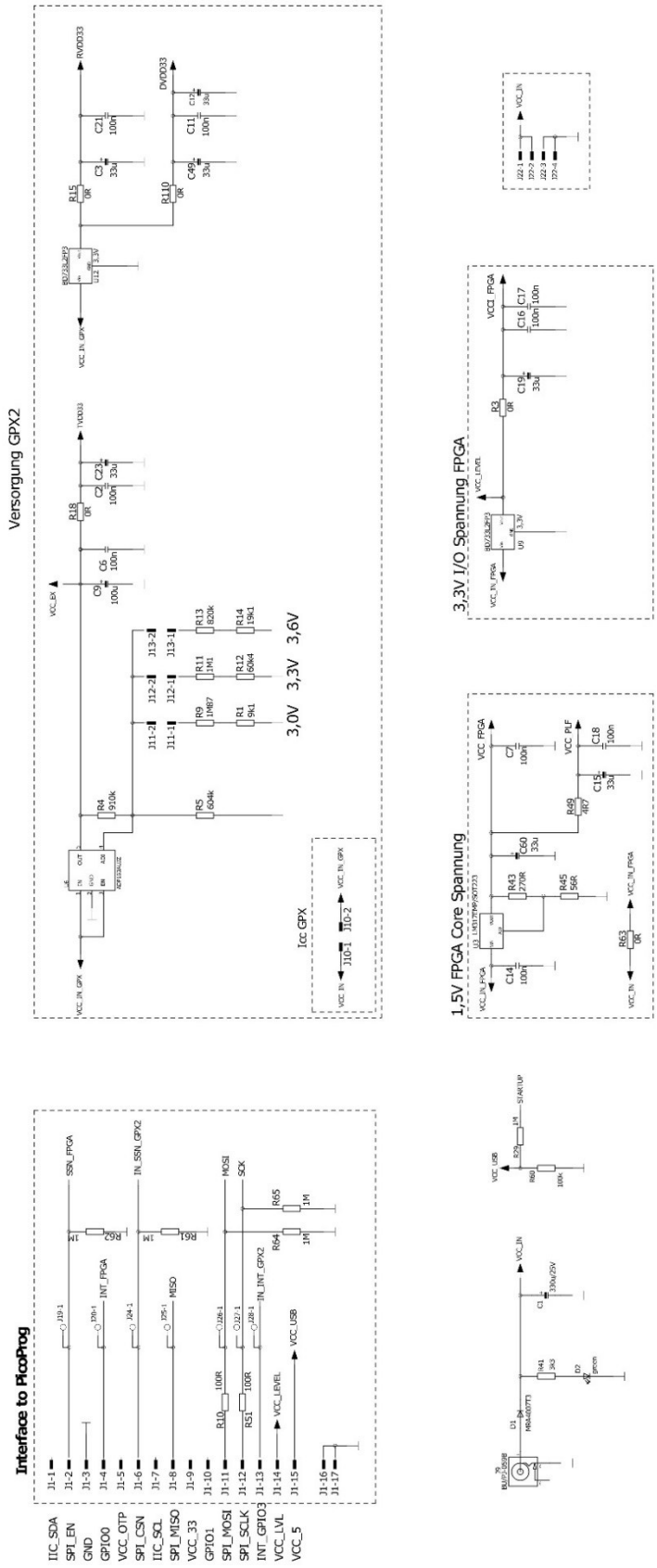


Figure 15: GP30-EVA BOARD Schematics 3

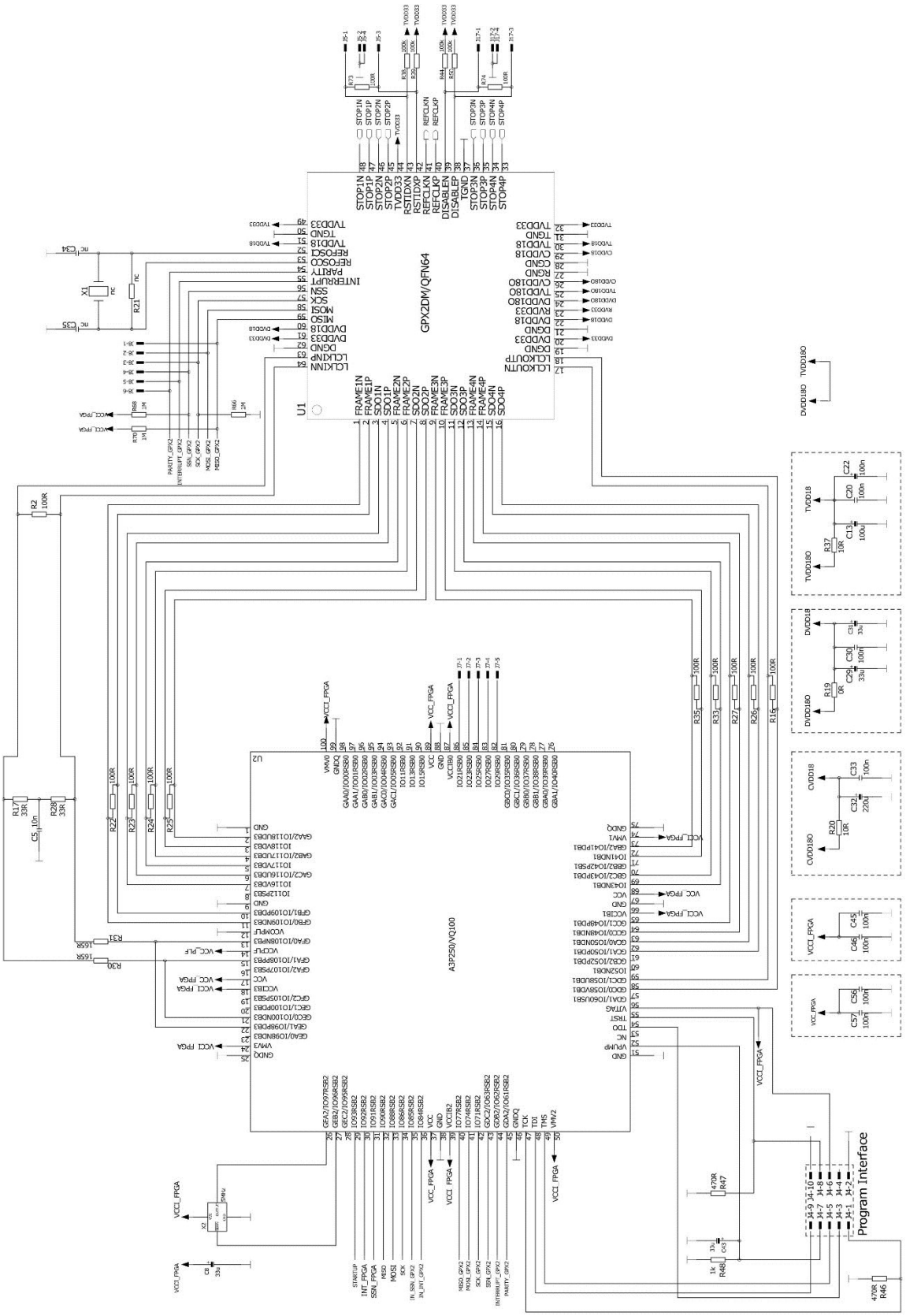


Figure 16: GPX2-EVA BOARD Layout: Top layer

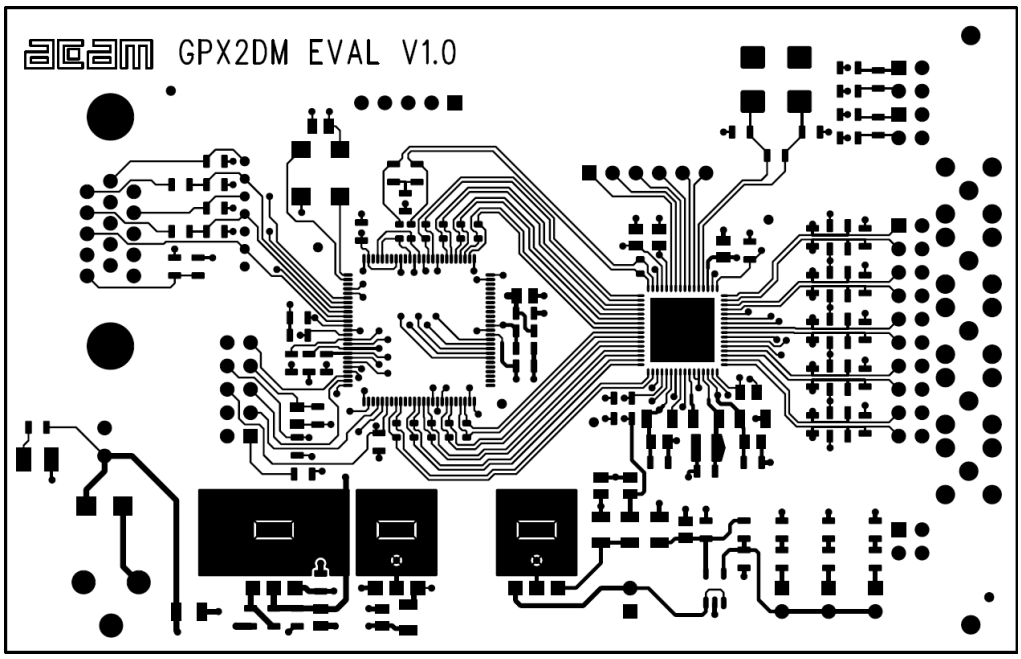


Figure 17: GPX2-EVA BOARD Layout: Layer2

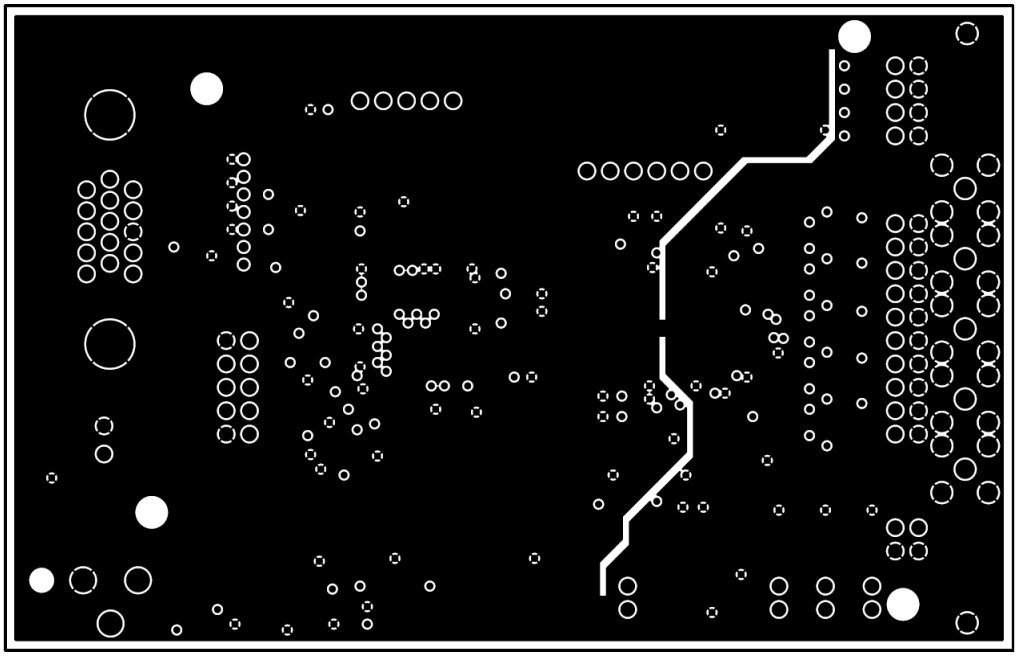


Figure 18: GPX2-EVA BOARD Layout: Layer 2

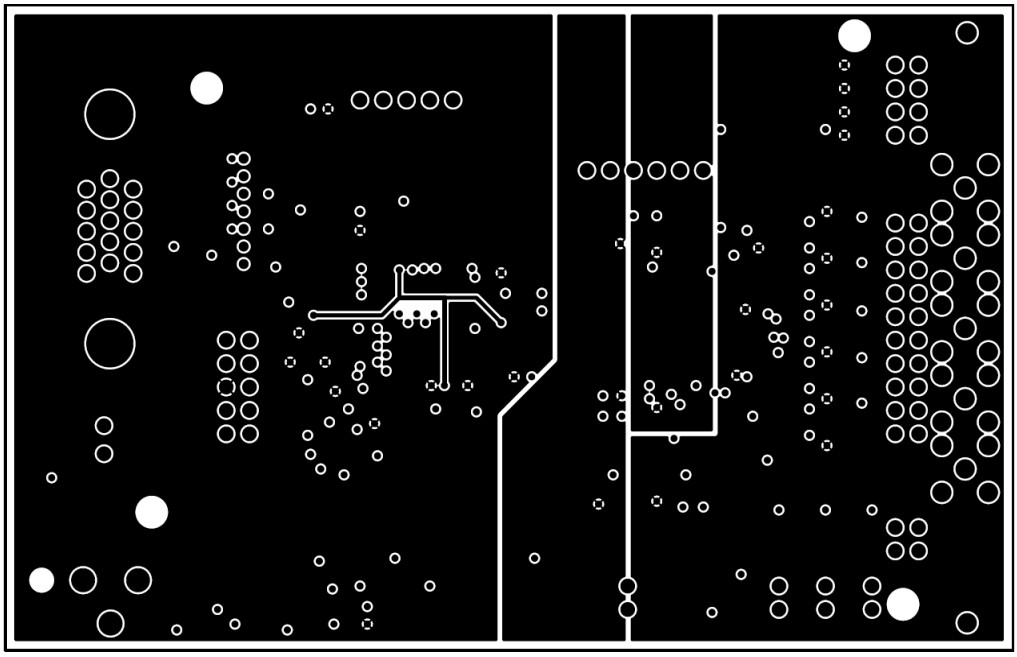


Figure 19: GPX2-EVA BOARD Layout: Bottom layer

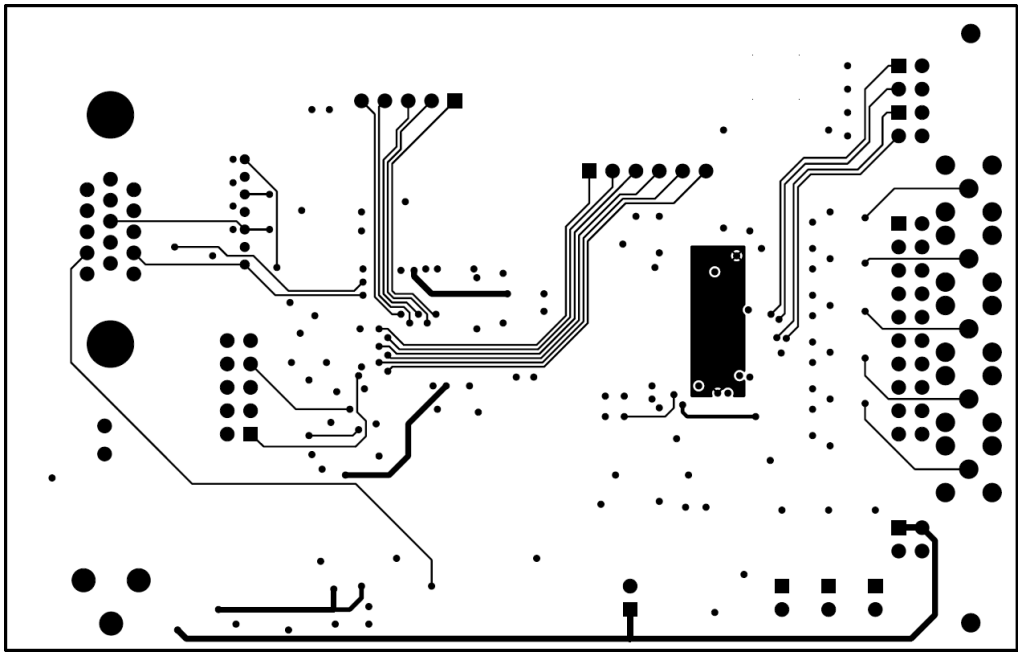


Figure 20: GPX2-EVA BOARD Layout: Assembly layer

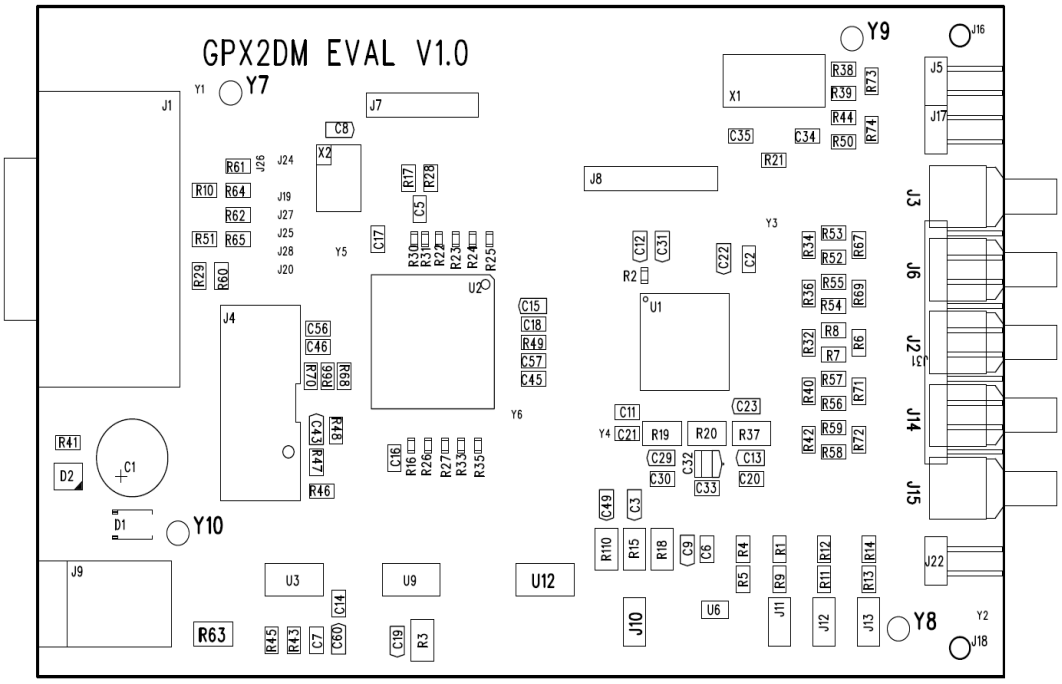


Figure 21: Bill of Materials for GP30-EVA BOARD

Item	Qty	Reference	Part Name	PART DESC	TYPE
2	1	U2	A3P250/VQ100	ProASIC3 Flash Family FPGA	A3P250VQG100
3	17	C2 C6 C7 C11 C14 C16 C17 C18 C20 C21 C22 C30 C33 C45 C46 C56 C57	C805,100n	CHIP-CAPACITOR	
4	1	C5	C805,10n	CHIP-CAPACITOR	
5	1	C1	ELKO/330u/25V	ELECTROLYTIC CAPASITOR	Radial 8mm Raster 3mm
6	1	C32	F95_B,220u	TANTAL	F950J227MBAAM1Q2
7	2	C9 C13	F95_P,100u	TANTAL	F950J107MPAAQ2
8	11	C3 C8 C12 C15 C19 C23 C29 C31 C43 C49 C60	F95_P,33u	TANTAL	F950J336MPAAQ2
9	1	D2	LED/HSMX-PLCC2,Grün	SURFACE MOUNT LED	
10	1	U3	LM317EMP/SOT223		
11	2	U9 U12	BD733L2FP3-CE2		BD733L2FP3-CE2
12	1	U6	ADP163AUJZ	CMOS Linear Regulator	ADP163AUJZ-R7
13	1	D1	MRA4007T3	DIODE	
14	1	X2	QSC/KXO-V97,5MHz	Crystal Oscillator	12.94354
15	10	R2 R16 R22 R23 R24 R25 R26 R27 R33 R35	R603,100R	CHIP-RESISTOR	
16	2	R30 R31	R603,165R	CHIP-RESISTOR	
17	1	R49	R805,4R7	CHIP-RESISTOR	
18	5	R6 R20 R37 R67 R69 R71 R72	R805,10R	CHIP-RESISTOR	
19	2	R17 R28	R805,33R	CHIP-RESISTOR	
20	1	R45	R805,56R	CHIP-RESISTOR	
21	2	R10 R51	R805,100R	CHIP-RESISTOR	
22	1	R14	R805,19k1	CHIP-RESISTOR	
23	1	R43	R805,270R	CHIP-RESISTOR	
24	2	R46 R47	R805,470R	CHIP-RESISTOR	
25	1	R48	R805,1k	CHIP-RESISTOR	

Item	Qty	Reference	Part Name	PART DESC	TYPE
26	1	R1	R805,9k1	CHIP-RESISTOR	
27	1	R41	R805,3k3	CHIP-RESISTOR	
28	1	R11	R805,1M1	CHIP-RESISTOR	
29	1	R12	R805,60k4	CHIP-RESISTOR	
30	1	R4	R805,910k	CHIP-RESISTOR	
31	1	R5	R805,604k	CHIP-RESISTOR	
32	1	R9	R805,1M87	CHIP-RESISTOR	
33	1	R13	R805,820k	CHIP-RESISTOR	
34	15	R7 R8 R38 R39 R44 R50 R52 R53 R54 R55 R56 R57 R58 R59 R60	R805,100k	CHIP-RESISTOR	
35	8	R29 R61 R62 R64 R65 R66 R68 R70	R805,1M	CHIP-RESISTOR	
36	8	R3 R15 R18 R19 R63 R110	R1206,0R	CHIP-RESISTOR	
37	4	J10 J11 J12 J13	ST/254_2	MULTI-PIN CONNECTOR	
38	1	J4	ST/254_10_2R_WANNE		1-1634688-0
39	1	J1	ST/DSUB15HD_ABG	MALE CONNECTOR DSUB15 ABG	
40	1	J9	BU/PJ-059B	DC Power Jack	PJ-059B
41	5	J2 J3 J6 J14 J15	ST/SMB_LPM_90	SMB CONNECTOR ABG	R114.665.000
42	1	U1	GPX2DM/QFN64	TDC-GPX2	

6 Ordering & Contact Information

Ordering Code	Part Number	Description
GPX2-EVA-KIT	220310001	TDC-GPX2 Eval Kit for QFN40 version including PICOPROG and cables
GPX2-EVA-BOARD	220310003	TDC-GPX2 evaluation board for QFN64

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8 Revision Information

Changes from previous version 0-02 to current revision 1-00 (2016-Oct-20)	Page
Transfer from preliminary to release version 1-00	

Note: Page numbers for the previous version may differ from page numbers in the current revision.
Correction of typographical errors is not explicitly mentioned.